FIG. 1
BACKGROUND ART

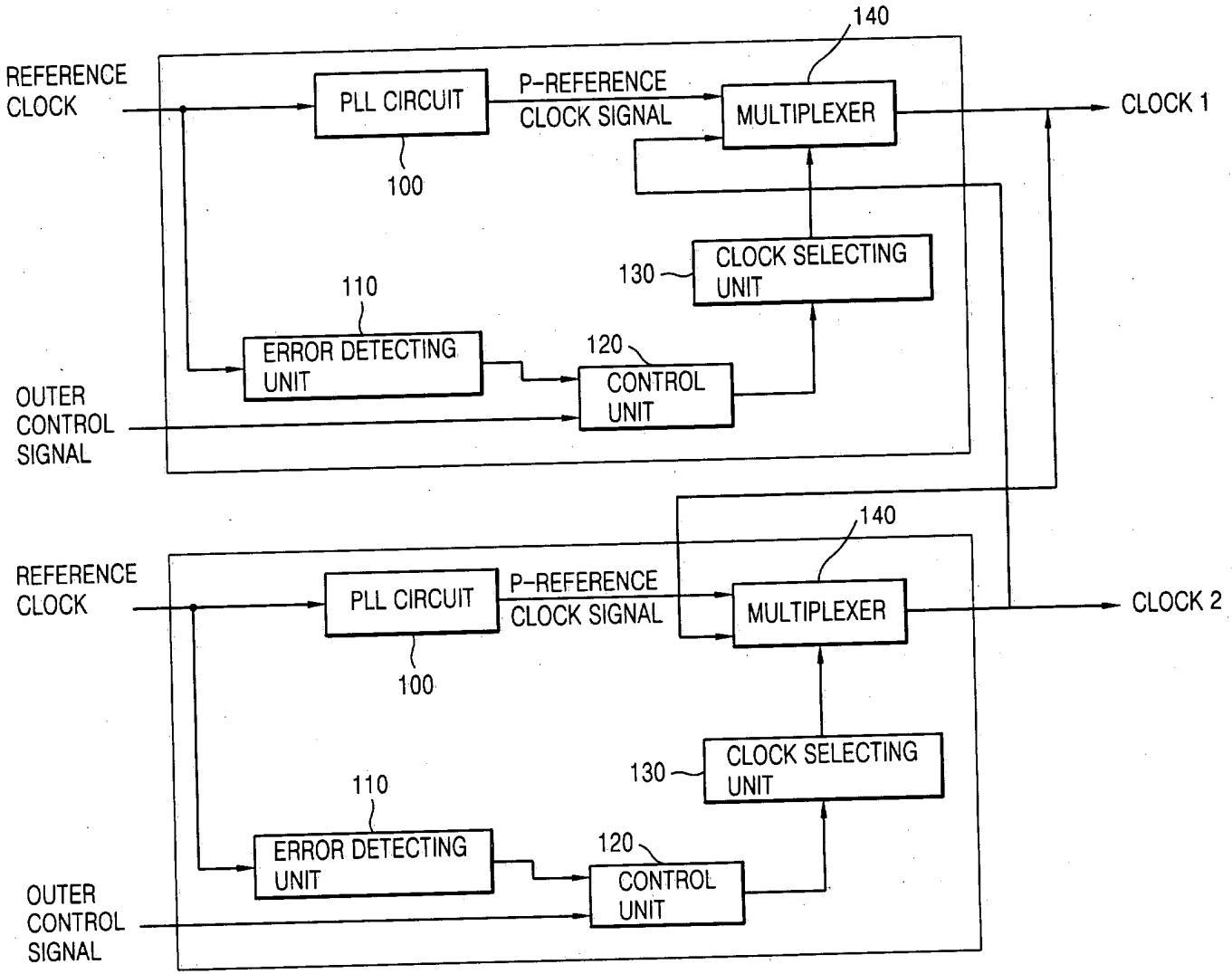


FIG. 2

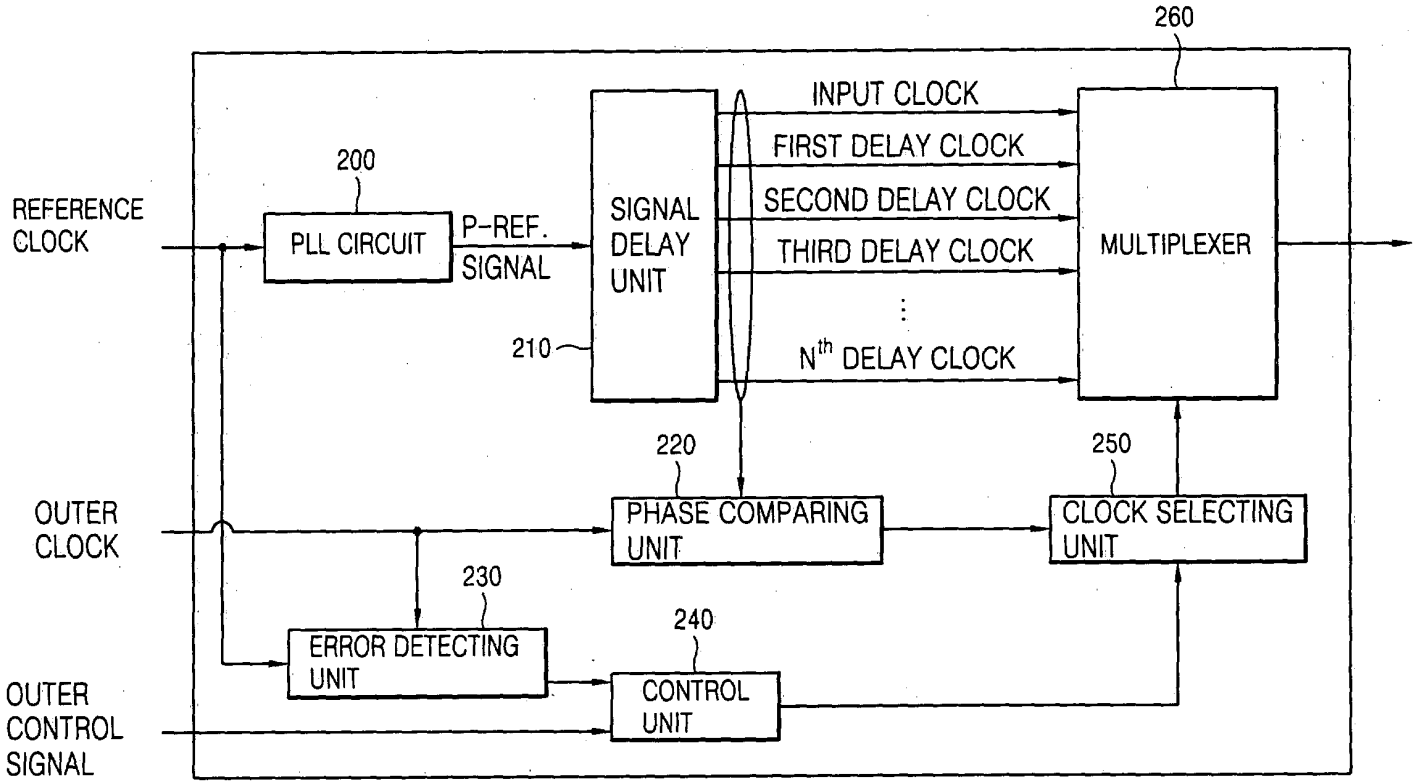

260
INPUT CLOCK
FIRST DELAY CLOCK
SECOND DELAY CLOCK
THIRD DELAY CLOCK
N^th DELAY CLOCK
MULTIPLEXER
200
REFERENCE CLOCK
PLL CIRCUIT
P-REF. SIGNAL
SIGNAL DELAY UNIT
210
220
PHASE COMPARING UNIT
250
CLOCK SELECTING UNIT
OUTER CLOCK
230
ERROR DETECTING UNIT
240
CONTROL UNIT
OUTER CONTROL SIGNAL

FIG. 3

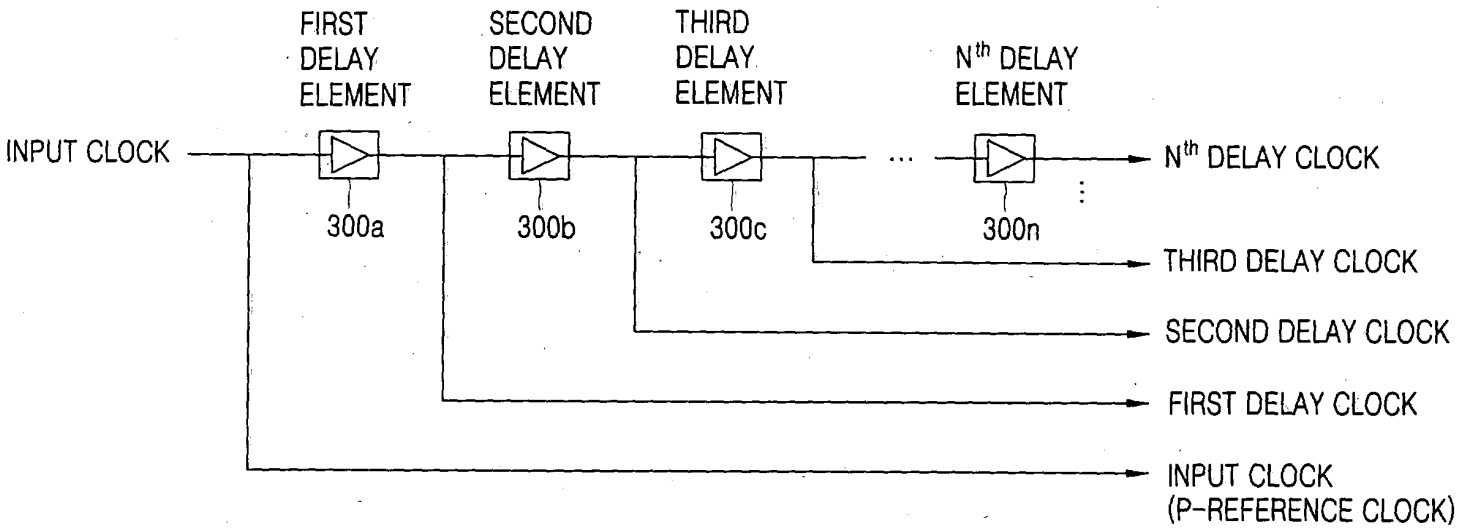

FIRST DELAY ELEMENT
SECOND DELAY ELEMENT
THIRD DELAY ELEMENT
N^th DELAY ELEMENT
INPUT CLOCK
300a
300b
300c
300n
N^th DELAY CLOCK
THIRD DELAY CLOCK
SECOND DELAY CLOCK
FIRST DELAY CLOCK
INPUT CLOCK
(P-REFERENCE CLOCK)

FIG. 4

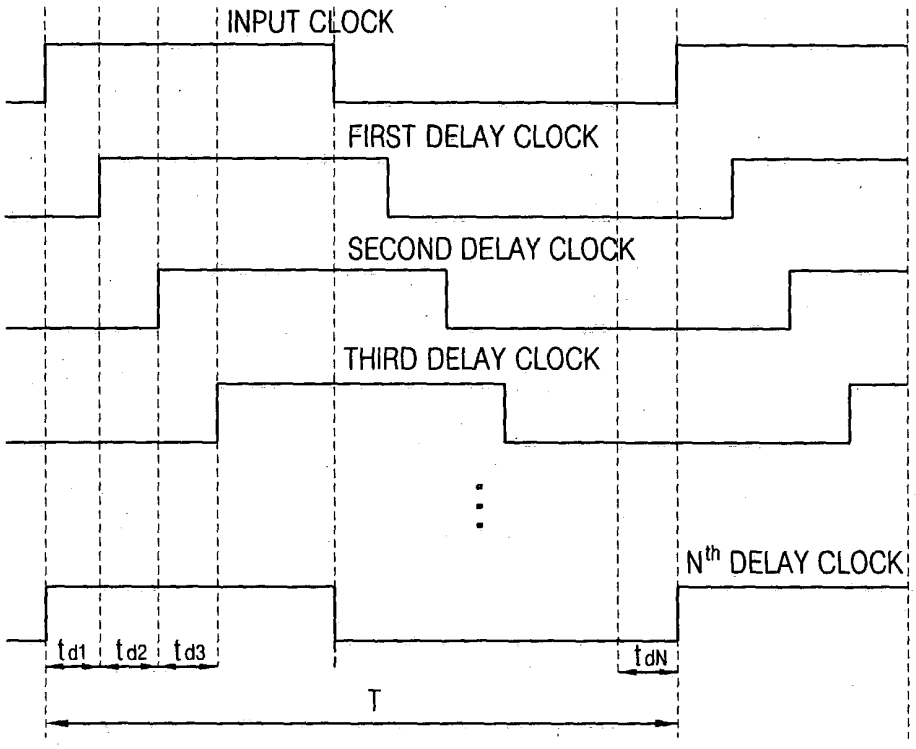

INPUT CLOCK
FIRST DELAY CLOCK
SECOND DELAY CLOCK
THIRD DELAY CLOCK
Nth DELAY CLOCK
td1
td2
td3
tdN
T

FIG. 5

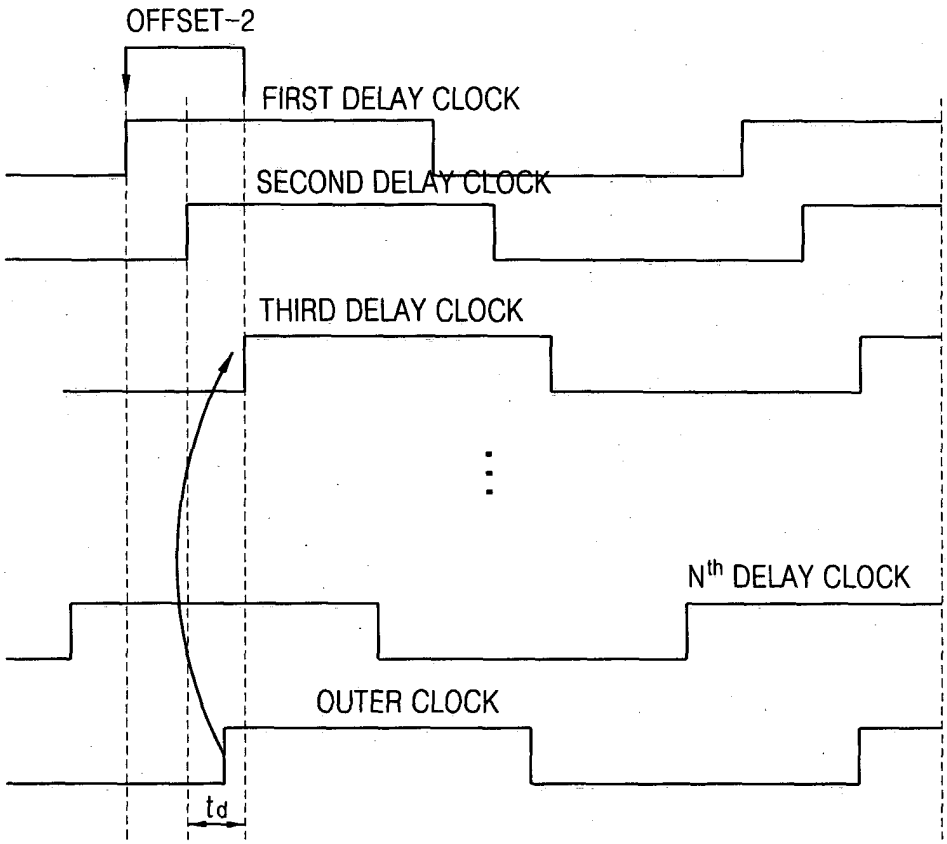

OFFSET-2
FIRST DELAY CLOCK
SECOND DELAY CLOCK
THIRD DELAY CLOCK
N^th DELAY CLOCK
OUTER CLOCK
td

FIG. 6

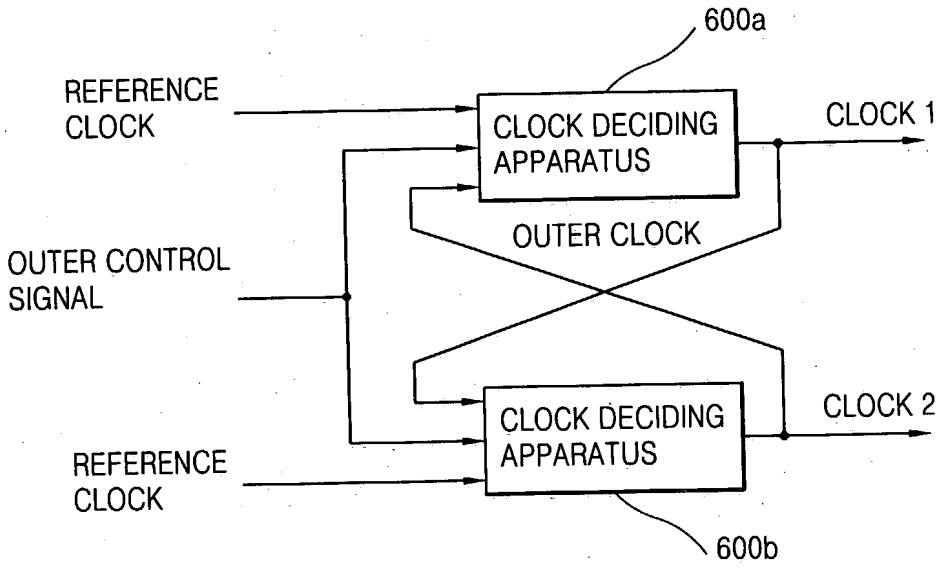
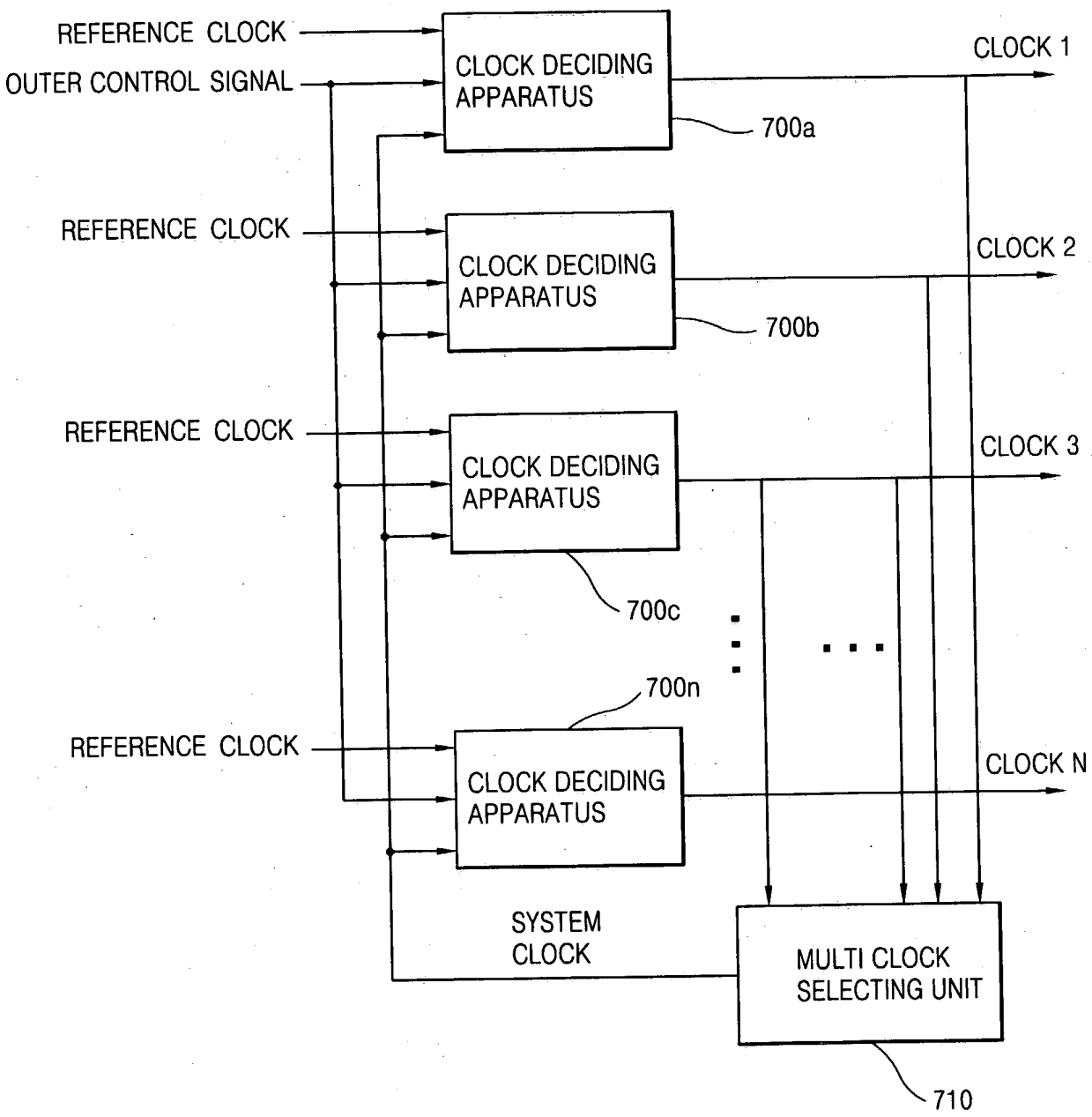

600a
REFERENCE CLOCK
CLOCK DECIDING APPARATUS
CLOCK 1
OUTER CLOCK
OUTER CONTROL SIGNAL
CLOCK DECIDING APPARATUS
CLOCK 2
REFERENCE CLOCK
600b

FIG. 7


REFERENCE CLOCK
OUTER CONTROL SIGNAL
CLOCK DECIDING APPARATUS
700a
CLOCK 1
REFERENCE CLOCK
CLOCK DECIDING APPARATUS
700b
CLOCK 2
REFERENCE CLOCK
CLOCK DECIDING APPARATUS
700c
CLOCK 3
700n
REFERENCE CLOCK
CLOCK DECIDING APPARATUS
CLOCK N
SYSTEM CLOCK
MULTI CLOCK SELECTING UNIT
710